Power section circuits are different than low-level analog and digital circuits. Large currents, high voltages and rapid rise-fall times are characteristics of such circuits. There is the additional requirement of accurately sensing millivolt-level voltages from these circuits. The physical layout of the printed circuit board is critical for these reasons. An incorrect board layout can result in poor circuit performance or it may not function at all even though all the parts are connected via circuit traces. Figure 1 shows a typical bipolar step motor power section:

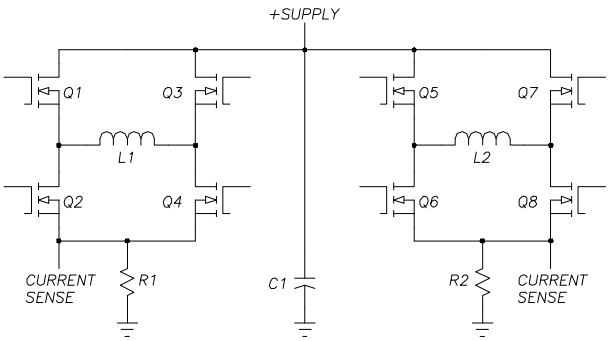

Fig. 1

Q1, Q2, Q3 and Q4 are the bridge n-channel power MOSFETs. R1 is the current sense resistor, L1 is one motor winding and C1 is the power supply bypass capacitor. Q5, Q6, Q7 and Q8, R2 and L2 forms the second motor winding bridge. All components pass the winding currents over the span of a switching cycle period. Additionally all components except L1 and L2 also pass the MOSFET intrinsic diode reverse recovery currents. These are narrow (< 200 nS) current pulses having an amplitude many times the motor winding currents. The current sense resistors R1 and R2 are usually very low value (< 50 milliohms) resistors to keep power dissipation reasonable. The voltages developed across these resistors range from a few millivolts to a few hundred millivolts and these voltages have to be measured accurately. This creates a very challenging environment requiring careful attention to board layout of the power section. Figure 2 shows how NOT to layout a power section:

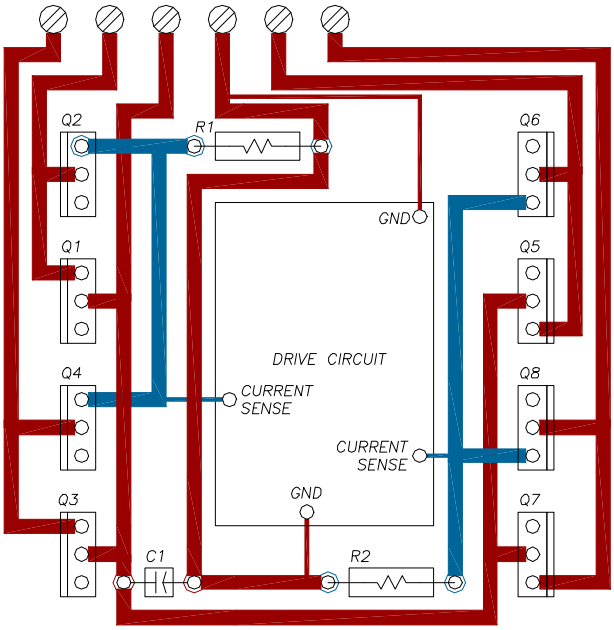

Fig. 2

The most common mistake is assuming board traces have zero resistance and inductance. This assumption is safe for most analog circuits and slower digital circuits. There will few negative consequences for circuits that use LM324 op-amps, LM339 comparators and 74HC00-series logic. Trace resistance and inductance cannot be neglected when the circuit uses power MOSFETs and carries large currents at high voltages.

The schematic in Figure 1 is correctly laid-out in Figure 2 if circuit traces had had zero resistance and inductance. Figure 3 adds actual trace resistances (Ra through Rj). These resistances change the performance of the circuit using this layout and it's not for the better.

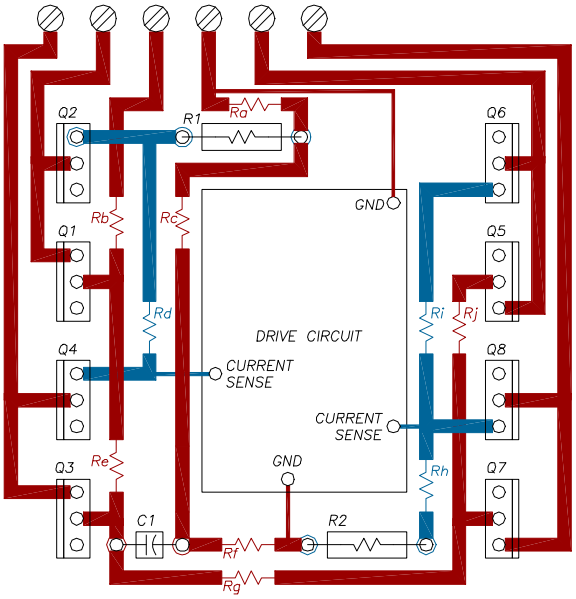

Fig. 3

Figure 3 represents the actual circuit when based on the resistances "added" by the board layout. Let's assume R1 and R2 are 0.05 Ohms and Ra through Rj are 0.01 Ohms. Figure 4 shows the same schematic in Figure 1 but now includes these "resistors".

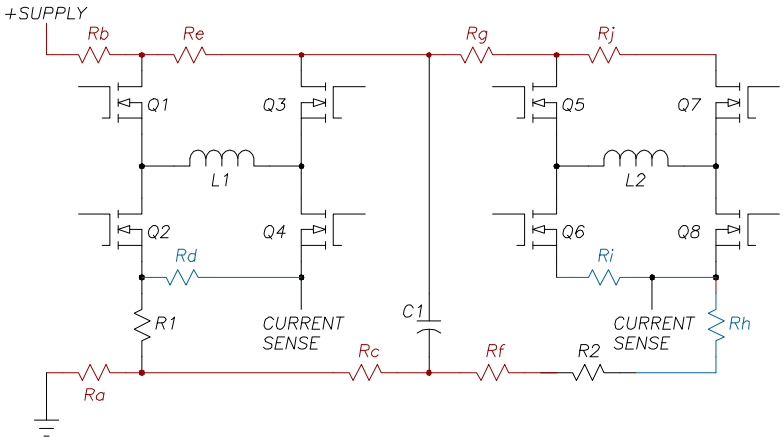

Fig. 4

From GND to Q4 source Ra, R1 and Rd are in series for a total of 0.07 Ohms. The current sense resistance GND to Q2 source is R1 and Ra or 0.06 Ohms. The PWM comparator reacts to voltage at the sense point (left CURRENT SENSE) so at a 350mV reference gives 5.83A through Q3, Q2 and 5A when current flows through Q1, Q4. This (a) doesn't give the expected 7A and (b) the waveform is distorted (+5.83A, -5.00A).

The situation for Q5, Q8 is 0.09 (Ra, Rc, Rf, R2 and Rh) Ohms giving +3.89A and 3.5A through Q7, Q6. 3.5A is only 50% of the expected 7A!

Things get far worse because the voltage drop across Ra partially adds the sensed currents thorough R1 and R2. The result is an audibly noisy drive because of the interaction between summed currents.

Rb, Re, Rg and Rj sums to 0.04 Ohms. A reasonable assumption is reverse recovery currents are 7 times the peak motor current of 7A. This makes the reverse recovery current about 50A. The voltage drop across 0.04 Ohms at 50A is 2V. More importantly is the dv/dt. The reverse current goes from zero to 50A in 10nS meaning the Q7 drain at the far end of the chain "sees" a dv/dt of –0.2V/ns. The MOSFET intrinsic drain to source diode is actually a parasitic bipolar NPN transistor, collector to drain, emitter to source. The base to emitter junction is nearly shorted-out so the base to collector junction forms this diode.

The problem is the base to emitter is only "nearly" shorted. The collector to base junction still retains its Miller capacitance. If the MOSFET drain to source sees a dv/dt exceeding 5v/ns, enough current is injected into the parasitic's base to emitter junction via the Miller capacitance to turn the NPN on. When this happens, the NPN avalanches and destroys the MOSFET. Having a significant resistance in the drain to +Vsupply path exposes the MOSFET to this failure mode. A trace that has 0.01 Ohm resistance will also have 1nH of inductance. Combined, the the dv/dt on the MOSFET drain can approach the danger value of 5V/ns.

Finally is the problem of GND pick-off points. The layout shows two, at the top and the bottom of the DRIVE CIRCUIT box. What lies between them is Ra, Rc and Rf totaling 0.03 Ohms. A 50A reverse recovery current will develop a 1.5V difference between these grounds. This introduces enough noise to cause mayhem in the low-level circuitry.

Figure 5 shows how to do a good power section board layout:

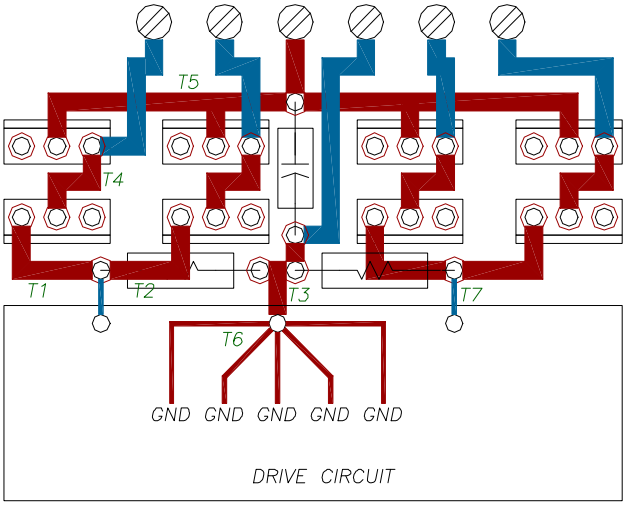

Fig. 5

T1 through T7 refer to circuit traces. Having T1 and T2 of equal length equalizes the motor current sense pick-off. T4 and the rest of the similar traces are kept very short all the way to the connector. T5 goes directly to C1 and minimizes trace resistance to the right and to the left. The bridge layout minimizes the traces that carry large currents to the absolute minimum.

Most important is what happens at T3.

R1, R2 and C1 must terminate as close to a single point as is possible. This is minimizes the trace resistance between these points. The GND reference to the rest of the drive circuit must be from this single point and nowhere else. The CURRENT SENSE pick-off points must be from the R1 and R2 pads.

Doing this forms a Kelvin connection. The idea behind a Kelvin connection is to accurately read a voltage across a sense resistor while canceling out the trace resistances. T3 terminates to a GND via in the DRIVE CIRCUIT. If the board layout is a double-sided one, all significant GND returns must be to this point. If the board is multi-layer, the via goes to the low-level circuit ground plane.

Figure 5 will work correctly but it's not an optimal layout. It uses fixed-width traces that leave a lot bare epoxy FR4 visible. A lot of copper gets needlessly etched away.

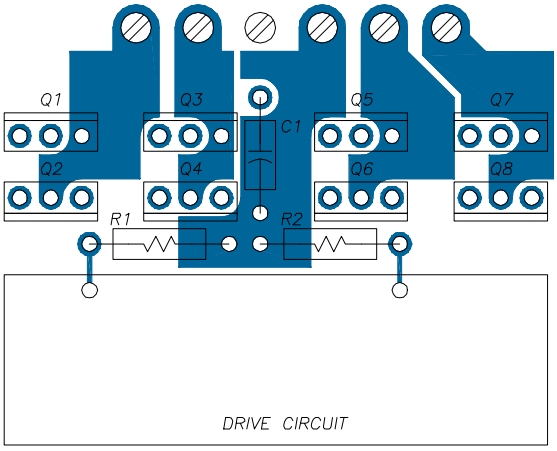

Fig. 6

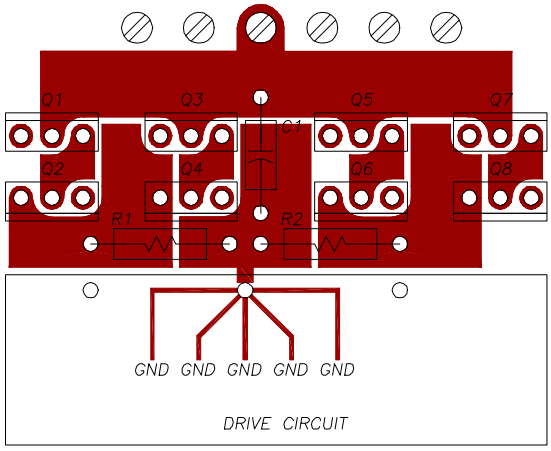

Fig. 7

Figures 6 and 7 shows the top and bottom copper respectively. Compare these against Figure 5. The layout has exactly the same connections but the copper fill area is much better. All that extra copper helps lower resistance and inductance in the critical areas of the power section. Fatten up the copper to the maximum possible. Copper that's been etched away cannot contribute to lowering trace resistance and inductance.

Signal section grounding and power distribution: The printed circuit board layout considerations are not as vital as for the power section but poor technique can still cause problems. Double-sided board layout is more critical than for a multi-layer board. It is much easier if when there are inner layers available for ground-plane and supply distribution. Figure 8 and figure 9 on the next page shows the bottom side copper for a double-sided plated-through hole example board. Both boards are laid-out for the same circuit and the parts location on the top copper is exactly the same.

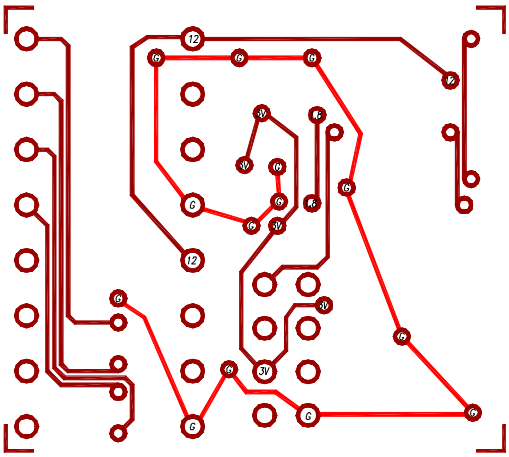

Fig. 8

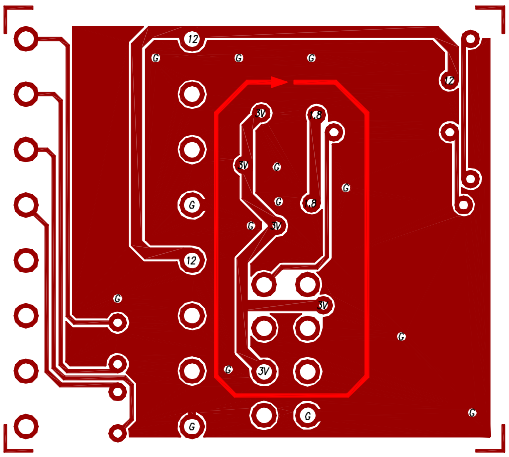

Fig. 9

Figure 8 shows how NOT to layout ground and power distribution. Highlighted in red is a snaked ground distribution. All grounds (every pad marked "G") are connected but they are like beads on a string. The same is true for the 1.8V, 3.3V and 12V power distribution (every pad marked 1.8, 3V and 12). There is bound to be a voltage difference between the head "G" pad and the tail "G" pad of this snake.

All the traces are the same width and an awful lot of copper has been etched away. If this is a low-frequency and low current analog or digital circuit then it probably will work. In reality this is a mixed analog-digital board using a CPLD and it certainly will not work properly because of noise issues caused by poor grounding and supply distribution.

Figure 9 shows the actual bottom copper. When only a 2-layer board is used, some special rules apply. Assign one layer as the main interconnection layer. Make most of your circuit signal trace connections on this layer. Use the other layer (bottom copper in this case) for signal trace routing only if absolutely necessary. Group the components on the signal layer according to the signal flow; if the signal flow is from A to B to C, then group components A, B and C on the board in that order. That will keep traces short and connections simple.

Use a "ring" approach to ground and supply distribution. In this example, the ground surrounds or rings the 3.3V power distribution. Note the highlighted red arrow that shows a continuous ground path around the 1.8V and 3.3V traces. Keep any other distribution traces to the periphery of the board (12V in this case) to maximize the ground-plane width.

Etch away as little copper as possible on this layer. Fatten-up all power supply traces.

To sum up, the rules are simple:

1) Keep circuit traces short: A 0.1" wide circuit trace has 0.01 Ohms per inch resistance at 25C (1.27mm wide trace is 0.01 Ohms per 25.4mm) for 0.5-oz copper. The 0.1" trace also has 1nH inductance per inch. Minimizing inductance in the MOSFET source to GND path is particularly important; reverse recovery currents can induce up to 1V per nH of inductance. 5V is sufficient to turn on a MOSFET that should be off. Place the power section components in close proximity to each other to keep traces short.

2) Make the circuit traces wide: Doubling the trace width halves its resistance. Consider using a "copper-pour" board layout technique to maximize copper in the power section of the board. Copper that is etched away is copper that cannot help lower trace resistance.

3) Place the high current components closely together. This keeps the high-current traces short, minimizing the effects of board circuit trace resistance and inductance.

4) Think of the board's copper foil as a sheet resistance (a continuous grid of many tiny resistors). This helps you see where the large circulating currents are. Place your signal pick-off points where little or no current is flowing on the copper-pour islands.

5) Use a Kelvin connection for the current sense resistors. Use a single-point ground pick-off to separate the grounds into high current and signal ground sections.

6) Use a multi-layer board if you can. Use the inner layers for ground-plane and power distribution. If a double-sided board is used, avoid "snaking" the ground and logic power distribution traces and use a ground "ring" to create a ground-plane.

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